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* Key

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1. A general-purpose VME module

Guo, Y.N.; Gao, Z.W.; Chang, M.C.; Li, H.H.; Wang, M.Z.;

[Nuclear Science, IEEE Transactions on](#)

Volume 50, Issue 5, Part 3, Oct. 2003 Page(s):1752 - 1755

Digital Object Identifier 10.1109/TNS.2003.818272

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(483 KB\)](#) [IEEE JNL](#)[Rights and Permissions](#)**2. The application of tiny triplet finder (TTF) in btev pixel trigger**

Wu, J.; Wang, M.; Gottschalk, E.; Shi, Z.;

[Real Time Conference, 2005. 14th IEEE-NPSS](#)

June 4-10, 2005 Page(s):108 - 112

[AbstractPlus](#) | [Full Text: PDF\(343 KB\)](#) [IEEE CNF](#)[Rights and Permissions](#)**3. A commodity solution based high data rate asynchronous trigger system for collider experiments**

Wang, M.; Jin Yuan Wu;

[Real Time Conference, 2005. 14th IEEE-NPSS](#)

June 4-10, 2005 Page(s):228 - 232

[AbstractPlus](#) | [Full Text: PDF\(244 KB\)](#) [IEEE CNF](#)[Rights and Permissions](#)**4. Integrated upstream parasitic event building architecture for BTeV level 1 system**

Jinyuan Wu; Wang, M.; Gottschalk, E.; Christian, D.; Li, X.; Shi, Z.; Pavlicek, V

[Real Time Conference, 2005. 14th IEEE-NPSS](#)

June 4-10, 2005 Page(s):607 - 611

[AbstractPlus](#) | [Full Text: PDF\(396 KB\)](#) [IEEE CNF](#)[Rights and Permissions](#)**5. Configurable area-IO memory for system-in-a-package (SIP)**

Wang, M.; Suzuki, K.; Dai, W.; Sakai, A.; Watanabe, K.;

[Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th](#)

18-20 Sept. 2001 Page(s):385 - 388

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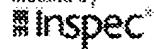
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E Waingold, M Taylor, V Sarkar, W Lee, V Lee, J ... - IEEE Computer, 1997 - aar.cs.ucdavis.edu
... The onerous compile times of our **multi-FPGA** based Raw prototype computer (see Section 6 ... The processor/network interface is shared between the two networks. ...
Cited by 287 - View as HTML - Web Search - SL Direct

[\[ps\] The Transmogrifier: The University of Toronto Field-Programmable System](#)

D Galloway, D Karchmer, P Chow, D Lewis, J Rose - Second Canadian Workshop on Field-Programmable Devices, ..., 1994 - eecg.toronto.edu
... Interface Board ... 4. TM-1 Interconnection Network In typical **multi-FPGA** boards, eg [Gokhale91], the wires that connect the FPGAs together are usually hard-wired ...
Cited by 22 - View as HTML - Web Search

[Logic Partition Orderings for Multi-FPGA Systems - group of 10 »](#)

S Hauck, G Borriello - FPGA, 1995 - doi.ieeecomputersociety.org
... Logic Partition Orderings for Multi-FPGA Systems ... This allows **multi-FPGA** partitioners to harness standard partitioning techniques. ...
Cited by 15 - View as HTML - Web Search

[A hardware implementation of a signaling protocol - group of 5 »](#)

H Wang, M Veeraraghavan, R Karri - Proc. of Opticom 2002 - ece.virginia.edu
... is that an out-of-band IP **network** will be ... timeslot pair and the outgoing interface/timeslot pair ... We used the WILDFORCE TM **multi-FPGA** reconfigurable computing ...
Cited by 14 - View as HTML - Web Search

[Scalable Pattern Matching for High Speed Networks - group of 6 »](#)

CR Clark, DE Schimmel - Proc. IEEE Symposium on Field-Programmable Custom Computing ..., 2004 - ieeexplore.ieee.org
... devices such as routers, switches, and **network interface** cards. At the upper end of the application spectrum, we envision larger, **multi-FPGA** systems operating ...
Cited by 8 - View as HTML - Web Search

[Hardware spiking neural **network** with run-time reconfigurable connectivity in an autonomous robot - group of 8 »](#)

D Roggen, S Hofmann, Y Thoma, D Floreano - Proc. 2003 NASA/DOD Conference on Evolvable Hardware, July, 2003 - doi.ieeecomputersociety.org
... I/O for the Khepera bus or user I/O • Stackable modules (**multi-FPGA** system sharing a ... UART and I/O) 2121 17.9ns • **Network interface** 163 7.83ns • Net. ...
Cited by 6 - View as HTML - Web Search

[\[ps\] Interconnect Synthesis for Reconfigurable Multi-FPGA Architectures - group of 7 »](#)

V Srinivasan, S Radhakrishnan, R Vemuri, J Wairath - bdd (Binary Decision Diagram) - ececs.uc.edu
... pipelined routing algorithm for **multi-FPGA** systems. ... through an api (Application Procedural Interface). ... that makes the interconnection **network** implement the ...
Cited by 6 - View as HTML - Web Search - SL Direct

[Implementation of BEE: a real-time large-scale hardware emulation engine - group of 7 »](#)

C Chang, K Kuusilinna, B Richards, RW Brodersen - FPGA, 2003 - portal.acm.org
... Figure 3: Various **multi-FPGA** interconnect topologies In light of the above two

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